

The listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) An integrated circuit device comprising:
a conductive contact in a hole in an interlevel dielectric layer;
a first spacer having a first dielectric constant on a side wall of the hole;
a second spacer having a second dielectric constant located between the first spacer and the side wall of the hole, wherein the first dielectric constant is less than the second dielectric constant; and
a contact pad in a substrate, wherein the conductive contact contacts the contact pad, wherein the first spacer extends along the side wall to contact the contact pad and wherein the second spacer does not contact the contact pad.
2. (Previously Presented) The integrated circuit device according to Claim 1, wherein the first spacer comprises silicon oxide and the second spacer comprises silicon nitride.
3. (Previously Presented) The integrated circuit device of Claim 1, wherein the thickness of the first spacer is in a range between about 10 Å and about 200 Å.
4. (Previously Presented) The integrated circuit device according to Claim 1, wherein the thickness of the second spacer is in a range between about 10 Å and about 300 Å.
5. (Previously Presented) The integrated circuit device according to Claim 1 further comprising:
a conductive line in the interlevel dielectric layer adjacent the first spacer opposite the conductive contact.
- 6-9. (Canceled)

10. (Previously Presented) An integrated circuit device comprising:
an integrated circuit substrate in which source/drain regions are formed;
a first interlevel dielectric layer which is formed on the integrated circuit substrate;
gate line patterns which are formed in the first interlevel dielectric layer;
contact pads which are present between adjacent gate line patterns in the first
interlevel dielectric layer and electrically connected to the source/drain regions;
a second interlevel dielectric layer which is formed on the first interlevel dielectric
layer, wherein contact holes, through which the contact pads are exposed, are formed in the
second interlevel dielectric layer;
first contact spacers which are formed along the side walls of the contact holes, the
first contact spacers being formed of silicon oxide;
second contact spacers which are formed of silicon nitride and formed on the first
contact spacers; and
contact plugs which are present in the contact holes between the second contact
spacers.

Claims 11-27. (Canceled)

28. (Previously Presented) The integrated circuit device of Claim 5, wherein the
conductive line comprises a gate line pattern.

29. (Previously Presented) The integrated circuit device of Claim 5, wherein the
conductive line comprises a bit line pattern.

30. (Previously Presented) The integrated circuit device of Claim 5, wherein the
conductive line comprises an interconnection line pattern.